Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims:

1. (Currently Amended) An integrated circuit ~~having logic blocks~~ comprising:

one or more logic blocks generating one or more system-operation signals at one or more system-operation clock rates;

a control unit for performing test and debug operations of said logic blocks of said integrated circuit;

a memory associated with said control unit, said memory holding instructions for said control unit; ~~and~~

a plurality of probe lines responsive to said control unit for carrying system-operation signals from ~~predetermined~~ a set of selectively enabled probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said memory[[,]];

an analysis engine implemented in the form of an on-chip logic analyzer having channels for capturing sequential snapshots of system-operation signals, said channels being coupled to said probe lines to move data captured at a probe point toward an end of a logic analyzer channel where data are stored in said memory so that said system-operation signals are retrievable,

wherein the set of selectively enabled probe points are selected from a set of pre-existing probe points coupled to the channels of said analysis engine and are selected by turning on enabling circuits,

and wherein said signal paths are capable of moving sets of said system-operation signals at at least one of said system-operation ~~system-operation~~ clock rates~~, said sets of~~

~~system operation signals stored in said memory so that said sets of system operation signals are retrievable~~.

2. (Previously Presented) The integrated circuit of claim 1 further comprising

a plurality of scan lines responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test signals and said test signal results stored in said memory so that said loading and retrieving operations are performed at one or more clock signal rates internal to said integrated circuit.

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~~3.~~ (Previously Presented) The integrated circuit of claim 2 further comprising

a unit coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

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~~4.~~ (Previously Presented) The integrated circuit of claim 2 wherein said scan lines comprise a first string of flip-flop connectors connected between a logic block and the remainder of said integrated circuit proximate said logic block, said flip-flop connectors providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode.

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~~5.~~ (Previously Presented) The integrated circuit of claim 2 wherein said scan lines comprise a second string of flip-flop connectors between elements of a logic block, said flip-flop connectors providing signal paths between said logic block elements in one mode and carrying test signals and test signal results in a second mode.

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~~6.~~ (Previously Presented) The integrated circuit of claim 1 wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying

system operation signals at predetermined probe points of said logic blocks in one mode.

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7. (Original) The integrated circuit of claim 6 wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode.

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8. (Original) The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying digital state system operation signals.

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9. (Original) The integrated circuit of claim 7 wherein at least some of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals reflective of analog conditions at said predetermined probe points.

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10. (Currently Amended) An integrated circuit comprising:

an interface for coupling to an external diagnostic processor;

~~a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;~~

an analysis engine implemented in the form of an on-chip logic analyzer having channels adapted to capture sequential snapshots of system-operation signals of said integrated circuit;

a plurality of probe lines coupled to said ~~unit~~ analysis engine for carrying said system operation signals from ~~predetermined~~ a set of selectively enabled probe points of said integrated circuit, wherein the selectively enabled probe points are selected from a set of pre-existing probe points coupled to the channels of said analysis engine and

turned on by enabling circuits, ~~wherein said probe lines comprise strings of storage elements providing signal paths from said probe points to said unit,~~ wherein said ~~signal paths~~ probe lines are capable of moving said sets of sequential system operation signals at one or more system operation clock rates; and

a memory coupled to said ~~unit~~ analysis engine and to said interface, said sets of sequential system operation signals being stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external processor at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals.

14 ~~11~~. (Previously Presented) The integrated circuit of claim 13 ~~10~~ wherein said unit further comprises trigger logic responsive to said system operation signals for initiating storage of a set of said system operation signals in said memory.

15 ~~12~~. (Previously Presented) The integrated circuit of claim 1 wherein said trigger logic is responsive to said system operation signals for terminating storage of said set of said system operation signals in said memory.

16 ~~13~~. (Original) The integrated circuit of claim 13 ~~10~~ wherein each of said probe lines comprises a string of programmable connectors providing a signal path for carrying system operation signals at predetermined probe points in one mode.

17 ~~14~~. (Original) The integrated circuit of claim 16 ~~13~~ wherein each programmable connector of said probe lines is programmed by a flip-flop connector, each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit

elements in one mode and carrying signals for programming said programmable connectors in a second mode.

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~~15~~. (Currently Amended) A method of operating an integrated circuit having logic blocks, a control unit, an analysis engine implemented in the form of an on-chip logic analyzer, a memory and a plurality of probe lines of said logic blocks, said method comprising:

operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

selectively enabling a subset of said probe lines responsive to said control unit, wherein the enabling of said probe lines is performed by turning on enabling circuits associated with said analysis engine, to capture and carry sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

moving, via channels of said analysis engine coupled to said probe lines, ~~said~~ captured sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit;[[,]]

storing said captured sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.

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~~16~~. (Previously Presented) The method of claim ~~15~~ wherein said system operation signals comprise sequential system operation signals.

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~~17~~. (Previously Presented) The method of claim ~~16~~ wherein said system operation signals comprise sets of sequential system operation signals.

18. (Previously Presented) The method of claim 15 wherein said integrated circuit has a plurality of scan lines of said logic blocks, said method further comprising

loading said memory with test signals and instructions for said control unit;

loading said scan lines responsive to said control unit with said test signals for said logic blocks at one or more clock signal rates internal to said integrated circuit;

operating said logic blocks at one or more clock signal rates internal to said integrated circuit;

retrieving test signal results from said logic blocks along said scan lines at one or more clock signal rates internal to said integrated circuit,

storing said test signal results in said memory at one or more clock signal rates internal to said integrated circuit; and

processing said stored test results signals in said control unit responsive to said stored instructions in said memory to perform test and debug operations of said logic blocks of said integrated circuit.

19. (Currently Amended) The integrated circuit of claim 10, wherein said memory is also coupled to a ~~said~~ system operation unit comprising logic blocks of said integrated circuit so that said memory unit may be accessed at least one of selectively ~~or~~ and simultaneously by said ~~data capture unit~~ analysis engine and said system operation unit.

20. (Previously Presented) The method of claim 1 wherein said system operation signals comprise sequential system operation signals.

21. (Previously Presented) The method of claim 20 wherein said system operation signals comprise sets of sequential system operation signals.

22. (Previously Presented) The method of claim 1 wherein said system operation signals are stored in said memory at one or more clock signal rates internal to said integrated circuit.